

Application Note

Application Information for the TDD1742T

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Summary:

This note covers the design of a phase locked loop based on the Philips TDD1742T (LOPSY) frequency synthesiser. A brief introduction to phase locked loops is given, followed by a derivation of the complete set of design equations.

Two worked examples are presented showing the use of the design equations for firstly a fast switching synthesiser and secondly a low noise synthesiser.

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Summary of Notation Used

The following terms are defined in the main body of the report as they are introduced, but are reproduced here for quick reference in alphabetical order. The terms are consistent throughout the report.

A	: prescaler division - $A/A + 1$ type prescaler	
BRA	: PC1 gain control	
BRB	: phase modulator gain control	
BRC	: analogue bias	
f	: modulating signal frequency	[Hz]
F_{osc}	: reference oscillator frequency	[Hz]
F_{out}	: VCO frequency	[Hz]
F_{ref}	: reference frequency at phase detector(s)	[Hz]
H(s)	: loop filter transfer function	
I_{bra}	: current through RA	[μ A]
I_{brb}	: current through RB	[μ A]
k	: gain applied to modulating signal for VCO	
K_d	: phase detector PC1 gain	[volts/rad]
K_{rc}	: gain of integrator for modulating signal applied to LOPSY $K_{rc} = 1/RC$	
K_v	: VCO gain	[rad/sec/volt]
K_v'	: VCO gain	[Hz/volt]
K_ϕ	: phase detector gain	[volt/rad]
M	: reference divider division ratio	
MEMEN	: memory/processor mode select	
N	: main divider division ratio	
n_0	: part of main divider chain	
n_1	: part of main divider chain	
n_2	: part of main divider chain	
OSC	: oscillator input	
P	: peak amplitude of modulating signal	[volt]
PC1	: analogue phase detector	
PC2	: digital phase comparator	
PE1	: program enable strobe	
PE2	: program enable strobe	
R_0	: part of reference divider chain	
R_1	: part of reference divider chain	
R_2	: part of reference divider chain	
RA	: PC1 gain setting resistor	[M Ω]
RB	: phase detector gain setting resistor	[M Ω]
s	: $j\omega$	
T_d	: modulator gain	[nsec/volt]
V_{dd1}	: digital supply voltage	
V_{dd2}	: digital 5V supply	
V_{dd3}	: analogue supply voltage	
V_o	: magnitude of integrated modulating signal	[volt]
XTAL	: crystal input	
ΔF	: peak deviation of VCO output	[Hz]
ϕ	: compensation for sample-and-hold in PC1	[rad]
Φ_m	: phase margin at loop bandwidth	[rad]
ω_n	: closed loop bandwidth of PLL	[rad/sec]

1. INTRODUCTION

This application note is intended as a guide to designing a phase locked loop based on the Philips TDD1742T (LOPSY) frequency synthesiser integrated circuit. The note starts with basic principles of phase lock, and progresses to cover the design of the complete loop using two worked examples. The design of the loop filter and implementing two-point modulation are covered in detail.

2. BASIC COMPONENTS OF THE PHASE LOCK LOOP

The purpose of a phase locked loop (PLL) is to lock two signals together in both frequency and phase. Typical applications include recovery of signals from noise and generation of frequencies from a known reference frequency. It is this second application that is of interest to us.

Our aim is to be able to generate one of a set of high frequencies to an accuracy determined by a low frequency reference clock. These frequencies are a fixed frequency apart - this is the channel spacing.

The block diagram of our circuit is shown in Fig.1. The circuit comprises a VCO which covers the range of frequencies we wish to tune over followed by a programmable divider chain, a reference oscillator followed by a fixed divider chain, a phase detector and a loop filter. The phase detector gives an error signal proportional to the difference in phase of the two input signals, so under in-lock conditions, these two inputs will be in phase and hence also at the same frequency. If we call this frequency F_{ref} , then, referring to Fig.1, we can say

$$F_{ref} = F_{osc} / M \quad (1)$$

where M = reference divider division ratio
 F_{osc} = reference oscillator frequency

and

$$F_{ref} = F_{out} / N \quad (2)$$

where N = main divider division ratio
 F_{out} = VCO frequency

thus

$$F_{out} = F_{osc} * N / M \quad (3)$$

Now, if we alter N by 1 we have

$$F_{out} = F_{osc} * (N + 1) / M \quad (4)$$

so our output frequency has shifted by

$$F_{osc} * (N + 1) / M - F_{osc} * N / M \quad (5)$$

i.e. by

$$F_{osc} / M \quad (6)$$

This is the same F_{ref} - see equation 1. We call F_{ref} the reference frequency and this is generally the same as the channel spacing, unless we require our generated frequencies to be offset by for example half a channel, when we would have to choose a reference frequency of half the channel spacing. We are able to select the output frequency desired by altering the value of the N divider as shown by the above equations. Normally, we will not need to alter the value of the M divider once we have set it to the required value.

We shall next consider the components in the PLL in turn.

2.1 The Reference Oscillator

This is a fixed frequency oscillator, generally of a high stability as it is this component that determines the frequency accuracy of our output signal.

2.2 The VCO

This is a variable frequency oscillator, the output frequency of which is determined by a control voltage input. The output frequency will have the same accuracy as the reference oscillator. It is desirable to have two buffered outputs - one for the divider input and one as the output from our PLL.

2.3 The Dividers

We have ascertained that the N divider needs to be programmable so that we can switch frequencies, and the M divider should allow us to select the desired reference frequency from our reference oscillator. In order to obtain all the desired division ratios in the N divider, the whole chain from VCO output to phase detector input needs to be programmable. These two frequencies are generally several orders of magnitude different, so the N divider is split into two separate divider stages, to take advantage of different semiconductor technologies. The high frequency part - or prescaler - is generally a dual modulus divider, that is it will divide by A or A + 1. The division is controlled by the subsequent part of the divider.

2.4 The Phase Detector

There are two requirements of the phase detector; firstly it must cover the full $\pm n$ radians phase range, and secondly it should have a good noise performance. The gain of the phase detector is expressed in volts/cycle or volts/radian. The output voltage is clearly limited by the supply voltage, so if we want to cover the full $\pm n$ phase range, we are limited to a gain of a few volts/cycle. However, for a good noise performance we really want a gain several orders of magnitude higher than this, but this will cause the phase detector to saturate at relatively low phase errors.

The solution is to have two phase detectors. The low gain phase detector can be used when we are significantly out of lock, and control can be handed over to the high gain phase detector when we are close to lock.

2.5 The Loop Filter

In order to make the loop gain correct and make the loop stable, an active filter is required. The design of the loop filter has a major effect on noise performance and switching times. Choosing a loop filter that gives a narrow loop bandwidth will give good noise performance at the expense of switching speed. The filter also should be designed so that the loop is properly damped, otherwise a poor switching response is obtained, or the loop may even be unstable.

3. USING THE TDD1742T - LOPSY

LOPSY incorporates the lower frequency part of the N divider, the M divider, the two phase detectors and also provides a modulation capability. The two phase detectors are the analogue phase detector PC1 and the digital phase comparator PC2.

3.1 PC1 Phase Detector

This is the high gain phase detector which produces an analogue voltage output proportional to the phase error between the M and N divider outputs. The gain depends on two factors - the reference frequency chosen, and the gain setting resistor described below. This phase detector has a sample-and-hold function internally which gives a time shift on the signal. This has an effect on the loop filter design; this is described in more depth below.

3.2 PC2 Phase Comparator

This is the low gain phase comparator which produces a digital positive or negative going pulse each reference cycle with a pulse width dependent on the phase error. During the remaining part of the cycle, the output is a high impedance, and the output is always high impedance if PC1 is in range. We shall call PC2 a phase comparator rather than a phase detector because of the digital nature of its output.

3.3 Connections to LOPSY

The number of external components required is small; we shall consider these first before moving on to the other loop blocks. Refer to Fig.2.

3.3.1 Power-up reset.

This sets LOPSY into a defined state of power-up. A simple RC delay is sufficient if the power supply has a reasonable rise-time. Care must be taken at power-up and also at power-down that V_{dd2} (5V supply) must never exceed V_{dd1} and V_{dd3} (7 to 10V supply). This is easily achieved if the 5V supply is generated by a regulator powered from the V_{dd1}/V_{dd3} supply.

3.3.2 Memory/Processor mode select.

At power-up, a decision is made as to whether LOPSY will be in memory mode or processor mode. In memory mode, LOPSY programs itself by outputting a series of addresses and reading back the corresponding set of data into its internal latches. This programming sequence is initiated at power-up and also on every active program enable edge. An active edge is any positive or negative going edge on either PE1 or PE2. In processor mode, the addresses and data must be externally supplied and each one latched with an active program enable pulse. An active program enable pulse is when PE1 and PE2 are in opposite states, e.g. PE1 high and PE2 low. Data and addresses should be stable for the duration of this condition, i.e. until PE1 and PE2 are returned to the same state.

The mode selection is made according to whether the MEMEN pin is high or low. If it is tied low, then LOPSY will enter processor mode; if it is pulled high via a suitable resistor, then LOPSY will enter memory mode and initiate a programming sequence. MEMEN should not be tied high as the memory mode programming sequence involves taking MEMEN low to provide a power-up signal for external ROMs or EPROMs. For details of the programming information see the relevant section below.

3.3.3 BRA bias setting resistor.

This controls the gain of the analogue phase detector. The gain is actually set by a current out of the BRA pin according to the following equation

$$PC1 \text{ gain } K_d = \frac{446 * I_{bra}}{F_{ref} * 1E3} \text{ volts/radian} \quad (7)$$

where F_{ref} = reference frequency in Hz
 I_{bra} = current in μA

I_{bra} has a design value in the range 5 to 30 μA . We can use the following equation to approximate RA from the value of I_{bra} out of the BRA pin

$$RA = \frac{V_{dd3} - 2.3}{I_{bra}} M\Omega \quad (8)$$

where I_{bra} = current in μA

In some cases it may be necessary to decouple RA with a suitable capacitor to reduce noise pickup.

3.3.4 BRB bias setting resistor.

This sets the gain of the internal modulator in a similar manner to the RA resistor. The modulator works by applying a voltage controlled delay between the main divider and the phase detector, so produces phase modulation. The time delay is given by approximately

$$\text{delay } T_d = \frac{909}{I_{brb}} \text{ nsec/volt} \quad (9)$$

where I_{brb} = current in μA

The design value for I_{brb} is in the range 3 to 25 μA . We can use the following equation to approximate RB from the value of I_{brb} out of the BRB pin

$$RB = \frac{V_{dd3} - 3.1}{I_{brb}} \text{ M}\Omega \quad (10)$$

where I_{brb} = current in μA

Alternatively, when $V_{dd3} = 7.5\text{V}$, the graph of modulator gain in Fig.3 can be used. In some cases it may be necessary to decouple RB with a suitable capacitor to reduce noise pick-up.

3.3.5 BRC Bias setting resistor.

This resistor provides bias setting for the remainder of the analogue circuitry and does not have any bearing on the loop parameters, so is non-critical in value. It can be calculated as for RB, and the current I_{brc} is normally chosen to be 20 μA . In some cases it may be necessary to decouple RC with the suitable capacitor to reduce noise pick-up.

3.3.6 Crystal oscillator.

The circuit shown in Fig.2 is a typical crystal oscillator based on the inverting amplifier at the OSC (input) and XTAL (output) pins. If an external oscillator is used, then it can be fed directly into the OSC input, bearing in mind that the switching threshold will be $V_{dd1}/2$. If this is inconvenient, then the external signal can be capacitively coupled to the OSC pin, and this input biased to $V_{dd1}/2$ by a high value (1 to 10M Ω) resistor connected between OSC and XTAL. In this condition the drive sensitivity is approximately 500mV peak to peak.

3.3.7 Main divider input.

As shown in Fig.2, the main divider input to LOPSY from the prescaler is capacitively coupled. LOPSY has a self-biasing input stage which requires a 1V peak to peak input signal. If the output from the prescaler provides proper logic levels for LOPSY then the capacitor can be omitted. The divider input switching threshold is at approximately $V_{dd1}/2$.

3.3.8 Data inputs/outputs.

The data inputs DB0-DB3 are MOS inputs, but with TTL logic levels, as are the PE1 and PE2 inputs. The address pins AB0-AB3 have the same input characteristics in processor mode, and are CMOS output level in memory mode.

3.4 Loop Filter Design

As has been stated above, the correct design of the loop filter is of considerable importance for the optimum performance of the synthesiser. A typical loop filter design is given in Fig.4, which also shows the time constants we must choose for the desired loop response. This filter works well for the analog phase detector PC1, but does not give the expected characteristic from the digital phase detector PC2 for practical realisations. The reason for this is that the output from PC2 is a narrow pulse of $\pm V_{dd3}/2$; when applied to the ideal version of the loop filter of Fig.4 this produces a large amplitude pulse superimposed on a small ramp from the integrating action of the feedback capacitor. Fig.5 shows the output from this circuit with an example of typical numeric values. Since a real op-amp cannot produce such a large amplitude swing nor a large slew rate, the output is far from ideal. This problem does not occur for the PC1 output since it is not a pulse output. The solution to this is the re-arranged version depicted in Fig.6, which has the final passive integrating stage moved to the PC1 and PC2 outputs; this alleviates the voltage swing and slew rate requirements of the op-amp. The drawback of this version is a lack of filtering of high frequency noise produced by the op-amp, but it does allow us to compensate for the time shift inherent in the PC1 phase detector mentioned briefly above. An additional integrating section can still be placed at the op-amp output provided it has a much higher frequency cut-off point than the loop bandwidth.

If noise performance is important, which is usually the case, it is necessary to choose an op-amp for the loop filter that has a good noise performance since this component can have more influence on the obtainable performance than LOPSY itself. If the final integrating stage after the op-amp is put in the circuit, then higher frequency noise from the op-amp will be filtered out, so is not of concern. On the other hand, low frequency noise will not be affected, so will cause low frequency fm on the VCO output. In general terms, bipolar op-amps tend to have better low frequency noise performance than CMOS types.

The design of the loop for PC2 (digital phase comparator) proceeds as follows: firstly we should choose the loop bandwidth ω_n . A suitable value is found from either noise considerations or from a bandwidth of the order of $2/\text{switching time}$. Next we must choose a suitable phase margin at the loop bandwidth.

A suitable value is 45° or $\pi/4$ radians - lower values give an underdamped characteristic, higher values an overdamped one. The three time constants are then calculated using

$$t3 = \frac{1}{\omega n} * \left\{ \frac{1}{\cos(\Phi m)} - \tan(\Phi m) \right\} \text{sec} \quad (11)$$

where ωn = closed loop bandwidth [rad/sec]
 Φm = phase margin [rad]

$$t2 = \frac{1}{\omega n^2 * t3} \text{sec} \quad (12)$$

$$t1 = \frac{K_v * K_\Phi}{N * \omega n^2} * \sqrt{\frac{1 + \omega n^2 * t2^2}{1 + \omega n^2 * t3^2}} \text{sec} \quad (13)$$

where K_v = VCO gain [rad/sec/volt]
 K_Φ = phase detector gain [volts/rad]

The values for C1, C2 can then be chosen fairly arbitrarily - if the subsequent calculated resistor values are unacceptably small or large then C1 and/or C2 can be altered. The necessary formula are (see Fig.4 for component identification).

$$R1 = t1 / C1 \quad (14)$$

$$R2 = t2 / C1 \quad (15)$$

$$R3 = t3 / C2 \quad (16)$$

If the type B loop filter is used then the following apply (see Fig.6 for component identification).

$$Ra = R1 / 2 \quad \text{or} \quad Ra = t1 / (2 * C1) \quad (17)$$

$$Ca = 4 * R3 * C2 / R1 \quad \text{or} \quad Ca = 2 * t3 / Ra \quad (18)$$

$$\text{and} \quad R2 = t2 / C1 \text{ as before}$$

We can do a similar process for PC1, but we need to take the sample and hold into account. The simplest method of doing this is to calculate the additional phase shift introduced at the loop bandwidth, and increase the desired phase margin by the same amount. The phase shift is given by

$$\phi = \frac{\omega n}{2 * F_{ref}} \text{ rad} \quad (19)$$

where F_{ref} = reference frequency [Hz]

since the effect of the sample and hold is a time shift, giving a phase shift proportional to frequency. The loop components can then be calculated as described for PC2 above.

If any other phase shifts are present, then they can be accounted for in the same way. For example, there may be additional poles in the circuit which will affect the loop response. The phase shift of these can be calculated at ωn , and this is then added to the desired phase margin. This is done in the second worked example below.

The two sets of results need to be combined since although we can choose R_a and C_a for each phase detector, for the type B, and only R_1 for the type A, they share the same remaining components. The best results are normally obtained by keeping the loop correct for PC1, and allowing the PC2 loop to have a higher phase margin than is necessary. This results in a slight degradation in switching time whilst on PC2 due to the loop being under-damped, but in practice a large proportion of the settling time is normally due to PC1, so this is acceptable. It is possible to increase R_a or R_1 (and decrease C_a correspondingly for a type B loop) to improve the switching time again, though care should be taken here as the loop will not be unconditionally stable if a large change is made. This increase in R_a or R_1 decreases the loop gain, and has the effect of decreasing the phase margin, which brings it closer to the desired value once more. Too much change will cause the open loop gain to cross the 0dB axis of the Bode plot with a slope of -12dB/octave rather than -6dB/octave.

Another method of combining the two sets of results is to choose the components so that C_1 is the same for both sets, thus giving different values for R_1 , and using the out-of-lock indicator to switch in the two different resistors required. The switches can be the 4066 CMOS switch type. This technique also allows us to choose different loop bandwidths for the two phase detectors to give a fast switching time with better noise performance than could be obtained otherwise. The technique is successful bearing in mind that with a low bandwidth for PC1 the ultimate settling time still be long, even though the coarse frequency steering by PC2 will be fast. It is best not to switch in different values for C_1 or C_2 since the stored charges in the capacitors when switching them in disturbs the loop, possibly sufficiently for it never to lock up.

3.5 Programming

There are eight registers that need to be programmed to give LOPSY the necessary main divider and reference divider information. In addition it is possible to completely disable the internal phase modulator if it is not required to eliminate noise pick-up. The main division ratio is given by

$$N = A * (128 * n2 + n1) + n0 \quad (20)$$

where $n0, n1, n2$ = main dividers in LOPSY

$$0 < n0 < 128$$

$$0 < n1 < 128$$

$$1 < n2 < 128$$

A = prescaler division ratio - the prescaler being a divide by A or A+1 type.

and the reference divider division ratio by

$$M = 4 * R0 * R1 * R2 \quad (21)$$

where $R0, R1, R2$ = reference dividers in LOPSY

$$R0 = 12/13/14/15$$

$$R1 = 9/5/6/7$$

$$R2 = 1/2/4/8$$

The bit map for the information is

address			data			
AB2	AB1	AB0	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0
0	0	1	n0.3	n0.2	n0.1	n0.0
0	1	0	R0.0	n0.6	n0.5	n0.4
0	1	1	n1.3	n1.2	n1.1	n1.0
1	0	0	R0.1	n1.6	n1.5	n1.4
1	0	1	n2.3	n2.2	n2.1	n2.0
1	1	0	M	n2.6	n2.5	n2.4
1	1	1	R2.1	R2.0	R1.1	R1.0

where n0.3 means bit 3 of n0 etc, bit 0 is least significant

M = 1 means modulator is enabled

The reference divider sections are mapped as follows:-

R2.1	R2.0	division
0	0	1
0	1	2
1	0	4
1	1	8

R1.1	R0.0	division
0	0	9
0	1	5
1	0	6
1	1	7

R0.1	R0.0	division
0	0	12
0	1	13
1	0	14
1	1	15

Programming is initiated whenever either the PE1 or PE2 pin changes state or at power-up in memory mode; LOPSY outputs the sequence of addresses. In processor mode, the addresses and data must be stable, and either PE1 or PE2 changed state to load that register. The register contents are not transferred to the dividers until register 7 (address = 111 binary) has been loaded.

3.6 Modulation

The peak deviation at the VCO output is given by the following expression, which is based on the system transfer function when the modulating signal is applied to the MOD pin of LOPSY

$$\text{deviation } \Delta F = P * \frac{s * T_d * F_{ref} * H(s) * K_{\Phi} * K_v}{s + H(s) * K_{\Phi} * K_v / N} \text{ Hz}$$

where P	=	peak amplitude of modulating signal [V]
s	=	j ω
T _d	=	delay in phase detector, from (9) [sec]
F _{ref}	=	reference frequency [Hz]
H(s)	=	loop filter transfer function
K _Φ	=	phase detector gain [V/rad]
K _v	=	VCO gain [rad/sec/V]
N	=	main divider division ratio
x	=	magnitude of x

We can see that at low frequencies (low s), the s term in the denominator is not significant, so can be ignored, giving us the expression below

$$\Delta F = P * 2 * \pi * f * T_d * F_{ref} * N \quad (23)$$

where f = modulating frequency [Hz]
other terms as in (22)

At higher modulating frequencies, the s term in the denominator dominates and so the equation becomes

$$\Delta F = P * T_d * F_{ref} * H(s) * K_{\Phi} * K_v \quad (24)$$

Since the magnitude of H(s) falls with increasing s, the deviation also falls. Therefore to achieve a proper modulation response, two measures must be taken. Firstly we must integrate the modulating signal before applying it to LOPSY to remove the 2 * π * f term in (22). Secondly, we must apply further modulation at some other point in the loop to make the modulation effective outside the loop bandwidth. If we apply the modulating signal to the VCO, then the equation for deviation becomes

$$\Delta F = P * \frac{s * K_v * k}{2 * \pi * (s + H(s) * K_v * K_{\Phi} / N)} \quad (25)$$

where K_v * k = VCO gain [rad/sec/V]

We use a different VCO gain here as our required deviation is normally much smaller than our VCO tuning range, so a much lower gain at this point is needed.

We can see that at low s, this tends to zero due to the increasing magnitude of the H(s) term in the denominator, and at high s this tends to

$$\Delta F = \frac{P * K_v * k}{2 * \pi} \quad (26)$$

Thus modulation applied to LOPSY is only effective below the loop bandwidth determined by H(s) and modulation applied to the VCO is only effective above the loop bandwidth.

If we now apply two point modulation by simply summing these two expressions taking into account the integrated version of the modulating signal applied to LOPSY, we have

$$\Delta F = \frac{P * K_v * k}{2 * \pi} * \frac{s + 2 * \pi * T_d * F_{ref} * H(s) * K_\Phi * K_{rc} / k}{s + H(s) * K_v * K_\Phi / N} \quad (27)$$

where K_{rc} = integrator gain (= 1/RC)
other terms as above

To make the modulation independent of the loop filter term, we want the numerator and denominator of the right part of this expression to be equal, that is

$$2 * \pi * T_d * F_{ref} * H(s) * K_\Phi * K_{rc} / k = H(s) * K_v * K_\Phi / N \quad (28)$$

Cancelling terms and re-arranging, and also substituting VCO gain in Hz/V rather than rad/sec/V gives

$$K_{rc} * T_d * F_{ref} * N = k * K_v \quad (29)$$

and our expression for deviation now becomes simply

$$\Delta F = P * K_v' * k \quad (30)$$

To implement the integrator, we can use either an active circuit based on an op-amp, or a simple passive RC section. At low frequencies, the active integrator will fail to operate correctly due to an output voltage limit, and the passive RC section ceases to integrate giving a low frequency roll-off on the modulation characteristic. The frequency at which these effects take place depends on the RC time constant, so this should be chosen bearing this in mind. The output of the integrator is given by

$$V_o = P * K_{rc} / (2 * \pi * f) \quad (31)$$

where V_o = integrator output [volts peak]

We have several gains to determine now; the necessary steps are

1. calculate k using (30) since we know ΔF , P and K_v'
2. choose a value for the RC integrator time constant. This gives us K_{rc} since $K_{rc} = 1/RC$
3. calculate RB to give the required T_d using (23), (9) and (10).

4. WORKED EXAMPLES

4.1 Fast Switching Synthesiser

4.1.1 Specification

As an example, we shall consider the design of a synthesiser with the following desired performance characteristics

output frequency	890 to 915MHz
loop filter output voltage swing	1 to 6V
reference oscillator frequency	12MHz
channel spacing	50kHz
modulation depth	$\pm 60\text{kHz peak}$
modulation signal amplitude	$\pm 500\text{mV peak}$
modulation signal frequency range	200Hz - 250kHz
VCO control voltage input capacitance	100pF
switching/lock time	<800µsec
supply voltage V_{dd1} , V_{dd3}	7.5V
reference suppression	better than -60dBC
noise performance - best obtainable	

Note that the noise performance is not expected to be very good because of the trade-off between noise performance and switching time.

4.1.2 Design

The VCO is chosen to cover the range 890 to 915MHz for the control range of 1 to 6 volts. To allow for changes of VCO gain and VCO centre frequency spreads, we will design for a frequency swing of 880 to 925MHz. The VCO gain K_v required is thus 7.5MHz/volt, or $K_v = 47\text{Mrad/sec/volt}$.

The prescaler is chosen to bring the VCO output below the maximum input frequency for LOPSY of 8.5MHz; a divide by 128/129 type prescaler is thus suitable, giving $A = 128$.

To give a good noise performance when locked up, we require a high gain for PC1. The gain is given by equations (7) and (8), and show that with a value of $270\text{k}\Omega$ for R_A we should obtain a gain of 196 volt/rad or about 1230 volt/cycle for PC1.

We now choose a loop bandwidth of 3kHz to satisfy the switching time requirement based on (2/switching time) allowing a margin for safety. Thus $\omega_n = 18850\text{ rad/sec}$.

We now calculate the total main division ratio from $910\text{MHz} / 50\text{kHz}$, giving $N = 18200$.

Knowing ω_n , K_v , N , F_{ref} , we can calculate the required loop filter. We will first do the calculations for PC1. We have an initial value of Φ_m of 45° , and we have to add a further 10.8° according to equation (19). Using this value for Φ_m of 55.8° , we find from (11), (12) and (13) that

$$t_3 = 16\mu\text{sec}$$

$$t_2 = 173\mu\text{sec}$$

$$t_1 = 3.68\text{msec}$$

We now choose values for C_1 and C_2 that will give reasonable values for R_1 , R_2 and R_3 . Suitable values are

$$C_1 = 2.2\text{nF} \qquad C_2 = 1.8\text{nF}$$

For a type A loop filter, we would have to add the VCO input capacitance to this value for C_2 , but we shall choose a type B as we require a good switching performance. This then gives the following using equations (14), (15) and (16)

$$R_1 = 1.67\text{M}\Omega \qquad R_2 = 78.6\text{k}\Omega \qquad R_3 = 9.06\text{k}\Omega$$

and then using equations (17) and (18) to convert to type B loop components and taking nearest values from the E24 series

$$R_a = 820\text{k}\Omega \qquad R_2 = 75\text{k}\Omega \qquad C_a = 39\text{pF}$$

We now repeat the design for PC2 using $\Phi_m = 45^\circ$, and obtain

$$t3 = 22.0\mu\text{sec}$$

$$t2 = 128\mu\text{sec}$$

$$t1 = 10.5\mu\text{sec}$$

We can choose different values for $t1$ and $t3$ from the results for PC1, but we do not have the freedom to select a different value for $t2$ unless we switch between two values for $R2$ as described in the loop filter description section above. The simplest solution to this is to use the higher value for Φ_m calculated for PC1. If we do this, then $t3$ and $t2$ are identical and $t1$ is reduced in proportion to the ratio of the gains of PC1 and 2. The gain of PC2 is simply $V_{dd1}/2\text{volts/cycle}$, i.e. 3.75 volts/cycle which gives the following results using the same procedure as before.

$$t1 = 11.2\mu\text{sec}$$

$$\text{hence } R1 = 5.10k\Omega$$

$$\text{thus } Ra = 2.4k\Omega, \text{ taking nearest E24 series value}$$

$$\text{and } Ca = 12nF, \text{ taking nearest E12 series value}$$

The next step is to design the modulator circuitry. We calculate k using equation (30) since we know ΔF , P and K_v' , giving us $k = 0.016$. This can be obtained using a simple resistive divider. In order to ensure that the output of the integrator does not overdrive the modulator in LOPSY, we must limit the output to around 1 volt peak-to-peak. The maximum output is given by equation (31), so from this we determine K_{rc} to be 1257, so we can choose

$$R = 36k\Omega \quad C = 22nF$$

We must now calculate the modulator gain required in LOPSY from equation (29), giving us a value for T_d of 104.4nsec . Using equation (9) we find $I_{brb} = 10.3\mu\text{A}$, which from equation (10) gives a value for RB of

$$RB = 430k\Omega$$

Finally we must calculate the programming information for LOPSY. Since we have $N = 18200$ and $A = 128$, the main divider sections require the following information according to equation (20) for a VCO frequency of 910MHz

$$n2 = 1$$

$$n1 = 14$$

$$n0 = 24$$

The reference frequency is obtained by choosing the following values according to equation (21)

$$R0 = 12$$

$$R1 = 5$$

$$R2 = 1$$

so using the tables in section 3.5 above, the information needed for these dividers is

$$R0.1 = 0 \qquad R0.0 = 0$$

$$R1.1 = 0 \qquad R1.0 = 1$$

$$R2.1 = 0 \qquad R2.0 = 0$$

giving the following data for the registers

address			data				
AB2	AB1	AB0	DB3	DB2	DB1	DB0	hex
0	0	0	0	1	0	0	4
0	0	1	1	0	0	0	8
0	1	0	0	0	0	1	1
0	1	1	1	1	1	0	E
1	0	0	0	0	0	0	0
1	0	1	0	0	0	1	1
1	1	0	1	0	0	0	8
1	1	1	0	0	0	1	1

This completes the design of our synthesiser. The complete circuit diagram is shown in Fig. 7, with LOPSY being in processor mode.

4.1.3 Performance

The above circuit was built, and some measures of its performance taken. A brief summary is

time to switch 100kHz	:	280µsec
time to switch 1MHz	:	450µsec
time to switch 10MHz	:	760µsec
reference frequency breakthrough	:	-53dBC
residual fm (in 30kHz bandwidth)	:	1.5kHz

A plot of the switching waveform is given in Fig.8 and shows the expected response of a single overshoot, returning to the correct level in the minimum time.

We can see that the reference frequency breakthrough does not meet our intended specification. In order to meet this we can put the final RC section after the loop filter as described in section 3.4 above, and re-calculate the loop filter components to take the additional phase shift of this section at the loop bandwidth into account in a similar manner to the method used to compensate for the sample-and-hold characteristic of PC1. Alternatively, if high frequency noise is not a problem, we can put an LC trap at the loop filter output. If this has a moderate Q then it is not too difficult to obtain sufficiently close values to remove a good proportion of the breakthrough, and the phase shift at the loop bandwidth is not sufficient to alter the damping significantly from the previously calculated values.

This was tried, and reduced the reference frequency breakthrough to -67dBC, whilst only have a small effect on the loop damping, making it slightly under-damped. The coil used had a Q of about 9.

4.2 Low Noise Synthesiser

4.2.1 Specification

This second example shows a synthesiser with a moderate switching speed, and a higher specification for noise performance. The desired characteristics are

output frequency	890 to 915MHz
loop filter output voltage swing	1 to 6V
reference oscillator frequency	7.2MHz
channel spacing	12.5kHz
modulation depth	± 6kHz peak
modulation signal amplitude	± 500mV peak
modulation signal frequency range	300Hz - 3.3kHz
VCO control volt input capacitance	100pF
switching/lock time	< 20msec
supply voltage V_{dd1} , V_{dd3}	7.5V
reference suppression	better than -70dBC
noise performance	< 30Hz residual fm

4.2.2 Design

For this example we will use the same VCO, prescaler and RA as the previous example. To meet the switching time we will choose a loop bandwidth of 200Hz. This also enables us to apply modulation to the VCO only, so the calculations for this will not be shown here. In order to ensure a good rejection of reference frequency breakthrough we will use the type B loop with an additional RC section between the filter and the VCO. If we choose a breakpoint of 800Hz, being 4 * loop bandwidth, then we will have an additional 24dB reference suppression and any op-amp noise will be band-limited to 800Hz. We will use R3 and C2 for the names of these components as in the type A filter. Hence we can choose

$$R3 = 4.3k\Omega \text{ and } C2 = 47nF$$

using E24 and E12 values respectively

We now calculate the phase margin required. This is made up from three components - the $\pi/4$ starting point, the effect of the sample-and-hold and the phase shift at the loop bandwidth of R3C2. The shift in an RC section is $\arctan(\omega CR)$ radians, and the S&H is given in (19), thus we have

$$\Phi_m = 0.785 + 0.050 + 0.249$$

$$= 1.084 \text{ rad/sec}$$

Although we are using the same RA as in the previous example, we can see from (7) that the gain of PC1 is higher. Equation (7) shows that

$$K_d = 687 \text{ volts/radian}$$

The gain of PC2 will remain the same of course. The parameters for the loop filter design are thus

$$\begin{aligned} \omega_n &= 1257 \text{ rad/sec} \\ N &= 72200 \\ K_v &= 47 \text{ Mrad/sec/volt} \\ F_{ref} &= 12.5 \text{ kHz} \\ \Phi_m &= 1.084 \text{ rad/sec} \\ K_d &= 687 \text{ volt/rad (PC1)} \\ &= 0.597 \text{ volt/rad (PC2)} \end{aligned}$$

Using the same procedure as before and designing for the PC1 loop, we find

$$\begin{aligned} t3 &= 198 \mu\text{sec} \\ t2 &= 3.20 \text{ msec} \\ t1 &= 1140 \text{ msec} \end{aligned}$$

We can choose $C1 = 470nF$ giving

$$\begin{aligned} C1 &= 470nF \\ R2 &= 6.8k\Omega \\ Ra &= 1.2M\Omega && \text{(for PC1)} \\ Ca &= 330pF && \text{(for PC1)} \\ Ra &= 1k\Omega && \text{(for PC2)} \\ Ca &= 390nF && \text{(for PC2)} \end{aligned}$$

The programming for a frequency of 910MHz is as follows

address			data				
AB2	AB1	AB0	DB3	DB2	DB1	DB0	hex
0	0	0	0	1	0	0	4
0	0	1	0	0	0	0	0
0	1	0	0	1	1	0	6
0	1	1	1	0	0	0	8
1	0	0	0	0	1	1	3
1	0	1	0	1	0	0	4
1	1	0	0	0	0	0	0
1	1	1	0	1	1	0	6

The circuit for this loop filter is given in Fig.9 - the remainder of the circuit is as shown in Fig.7.

4.2.3 Performance

A brief summary of the performance obtained is

time to switch 20MHz : 25msec
reference frequency breakthrough : not measurable (<-90dBC)
residual fm (in 30kHz bandwidth) : 17Hz unweighted
: 11Hz CCITT weighted

The switching time does not meet our intended specification. This is due to the underdamped PC2 loop. By making the following adjustments as described in section 3.4 above, the switching time was reduced

$$Ra = 1.8k\Omega \quad (\text{for PC2})$$

$$Ca = 220nF \quad (\text{for PC2})$$

time to switch 20MHz : 20msec
reference breakthrough and residual fm unaffected.

Note that the VCO chosen for this application should itself be a low noise device as the loop can only reduce VCO noise below the loop bandwidth. The spectrum plots of reference frequency breakthrough and close-in noise performance are given in Figs.10 and 11 respectively.

5. CONCLUSIONS

The basic principles of a frequency sythensiser have been covered. The use of LOPSY in such a frequency locked loop has been discussed in general terms covering programming, design of the loop filter and modulation with details of the necessary design equations. Two worked examples have been used to give an idea of the necessary design procedure, and some performance figures given.

6. REFERENCES

1. TDD1742T data sheet, February 1987
2. Ulrich L. Rohde; Digital PLL Frequency Synthesisers Theory and Design.
3. N.M.W. Oatley; 900MHz Frequency Synthesiser for Cellular Radio applications using the TDD1742T (LOPSY), MCO8501.
4. P.J. Hart; 'LOPSY' - Low Power Frequency Synthesiser Application Information, MCO8302.

APPENDIX 1

Summary of Modulation Design Equations

Modulation is applied to the VCO via an attenuator, and to LOPSY via an integrator.

The following terms are used, and have the same definition as in the main body of the report:-

VCO gain	: K_v'	[Hz/volt]
Modulator gain	: T_d	[sec/volt]
Modulator gain setting current	: I_{brb}	[μ A]
Modulator gain setting resistor	: R_B	[Ω]
Main divider & prescaler division ratio	: N	
VCO modulation signal attenuator gain	: k ; $k \ll 1$ normally	
LOPSY modulation signal integrator gain	: K_{rc} ; $K_{rc} = 1/RC$	[1/sec]
Output from integrator (peak)	: V_o	[volts]
Modulation signal magnitude (peak)	: P	[volts]
Modulating signal frequency	: f	[Hz]
Modulation depth (peak)	: ΔF	[Hz]
Reference frequency	: F_{ref}	[Hz]

The parameters are chosen by the following steps:-

1. Calculate k using equation (30) to give required deviation at VCO output.
2. Calculate K_{rc} time constant for the integrator, so that maximum output from the integrator is not significantly greater than 1 volt peak-to-peak using (31).
3. Calculate modulator gain required using (29). If this is out of the acceptable range then K_{rc} will have to be adjusted.
4. Calculate I_{brb} to give the required T_d using (9).
5. Calculate R_B resistor value to give this I_{brb} using (10).

Note that large deviations at small reference frequencies will cause the requirements of 2 and 3 above to be irreconcilable

The equations are repeated below for convenience.

$$\Delta F = P * K_v' * k \quad (30)$$

$$V_o = P * K_{rc} / (2 * \pi * f) \quad (31)$$

$$K_{rc} * T_d * F_{ref} * N = k * K_v' \quad (29)$$

$$delay T_d = \frac{909}{I_{brb}} \text{ nsec/volt} \quad (9)$$

$$RB = \frac{V_{dd3} - 3.1}{I_{brb}} M\Omega \quad (10)$$

note RB in MΩ

APPENDIX 2

Summary of Loop Filter Design Equations

The following terms are used, and have the same definition as in the main body of the report:-

VCO gain	: K_v	[rad/sec/volt]
Phase detector gain	: K_ϕ	[volt/rad]
Phase detector gain setting current	: I_{bra}	[μA]
Phase detector gain setting resistor	: R_A	[Ω]
Main divider & prescaler division ratio	: N	
Reference frequency	: F_{ref}	(Hz)
Phase margin at loop bandwidth	: Φ_m	[rad]
PC1 S&H phase compensation	: ϕ	[rad]
Closed loop natural frequency	: ω_n	[rad/sec]
Loop filter time constants	: t_1, t_2, t_3	[1/sec]
Type A loop filter components	: R_1, R_2, R_3, C_1, C_2	
Type B loop filter components	: R_a, C_a, R_2, C_1	

To calculate the loop filter components, the following steps are necessary, assuming the PC1 (analogue) detector loop parameters:-

1. Choose either type A or type B loop filter.
2. Modify Φ_m to take the sample-and-hold into account using (19).
3. Calculate I_{bra} to give required PC1 gain using (7).
4. Calculate R_A to give this I_{bra} using (8).
5. Calculate t_3 using (11)
6. Calculate t_2 using (12)
7. Calculate t_1 using (13)
8. Choose values for C_1, C_2 .
9. Calculate R_1 using (14)
10. Calculate R_2 using (15)
11. Calculate R_3 using (16)
12. If type B filter is used then
 1. calculate R_a using (17)
 2. calculate C_a using (18)

The process is the same for PC2 (digital) phase comparator except that step 2 is not relevant. The two sets of results need to be combined which can be done by either switching different resistors in using the out of lock indicator to control the switches, or by allowing the PC2 loop to have the same phase margin as the modified value used in the calculations for PC1.

The equations are repeated below for convenience.

$$\Phi = \frac{\omega n}{2 * F_{ref}} \text{ rad} \quad (19)$$

$$PC1 \text{ gain } K_d = \frac{446 * I_{bra}}{F_{ref} * 1E3} \text{ volts/radian} \quad (7)$$

$$RA = \frac{V_{dd3} - 2.3}{I_{bra}} M\Omega \quad (8)$$

$$t3 = \frac{1}{\omega n} * \left\{ \frac{1}{\cos(\Phi_m)} - \tan(\Phi_m) \right\} \text{ sec} \quad (11)$$

$$t2 = \frac{1}{\omega n^2 * t3} \text{ sec} \quad (12)$$

$$t1 = \frac{K_v * K_\Phi}{N * \omega n^2} * \sqrt{\frac{1 + \omega n^2 * t2^2}{1 + \omega n^2 * t3^2}} \text{ sec} \quad (13)$$

$$R1 = t1 / C1 \quad (14)$$

$$R2 = t2 / C1 \quad (15)$$

$$R3 = t3 / C2 \quad (16)$$

$$Ra = R1 / 2 \quad \text{or} \quad Ra = t1 / (2 * C1) \quad (17)$$

$$Ca = 4 * R3 * C2 / R1 \quad \text{or} \quad Ca = 2 * t3 / Ra \quad (18)$$

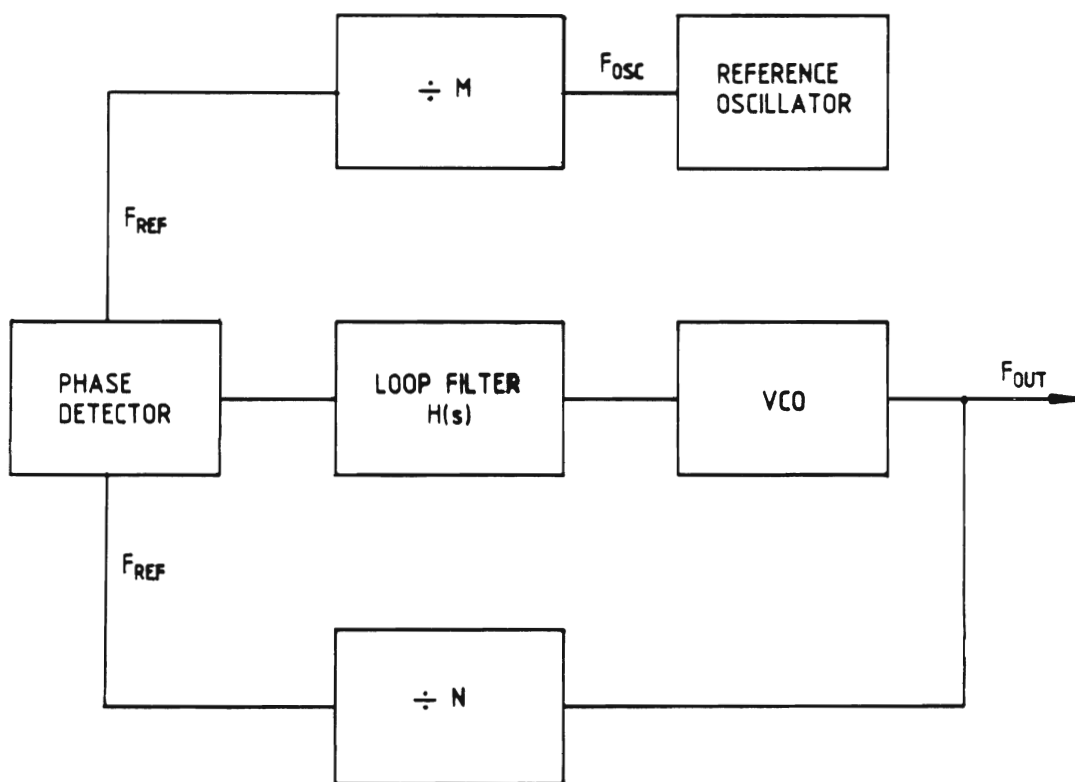


FIG. 1. BLOCK DIAGRAM OF PLL.

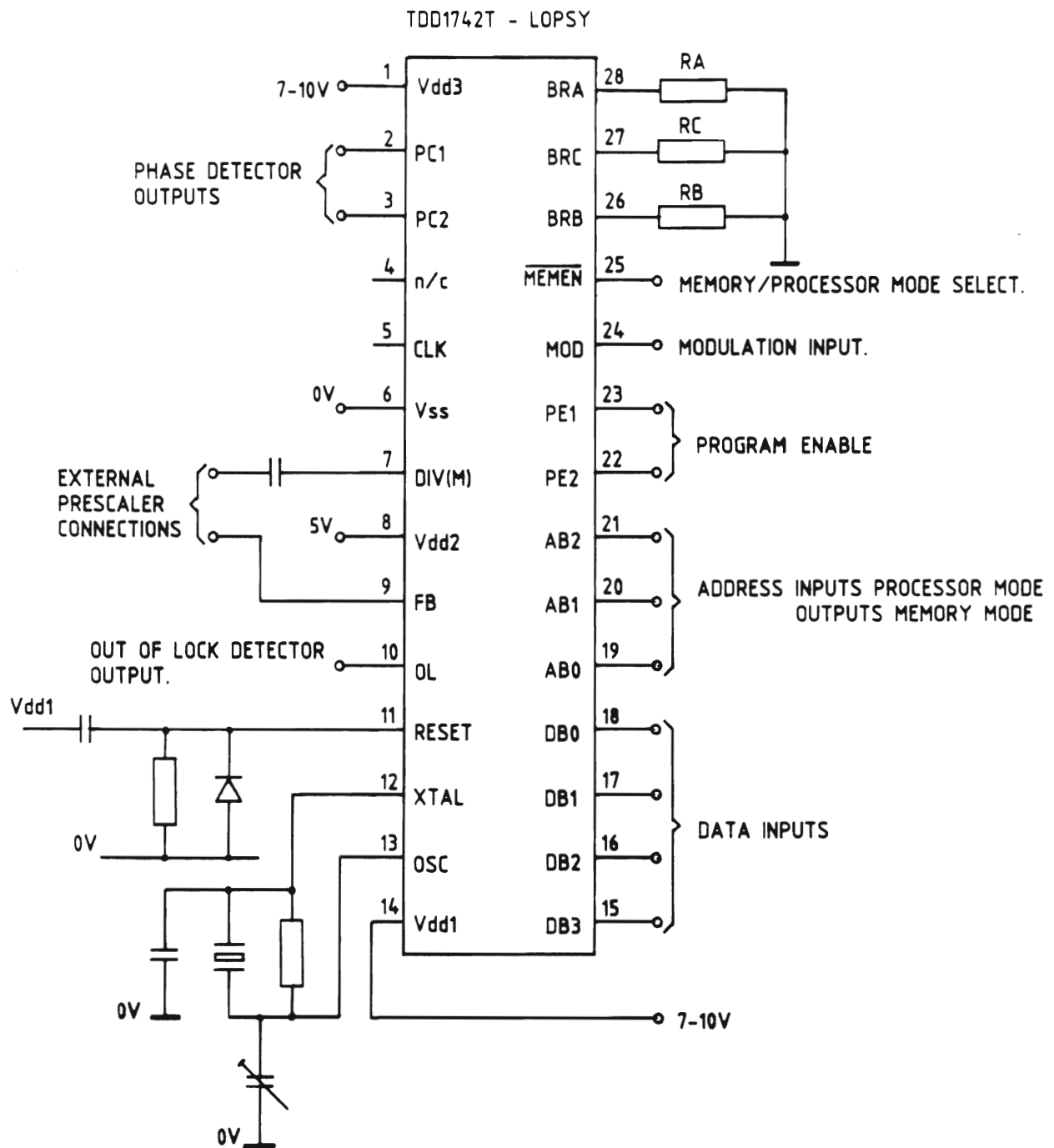


FIG. 2. CONNECTIONS TO LOPSY

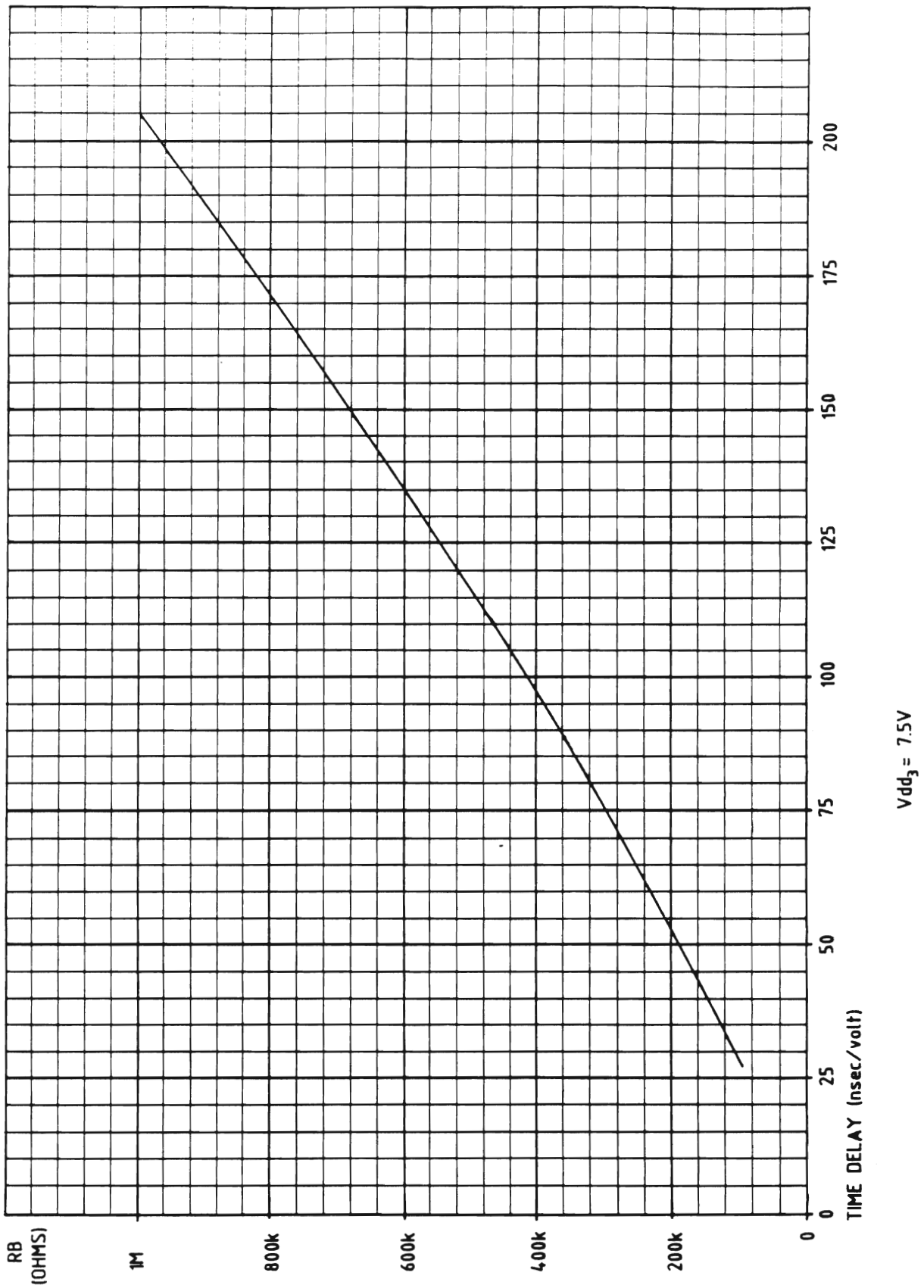


FIG. 3. GRAPH OF MODULATOR GAIN.

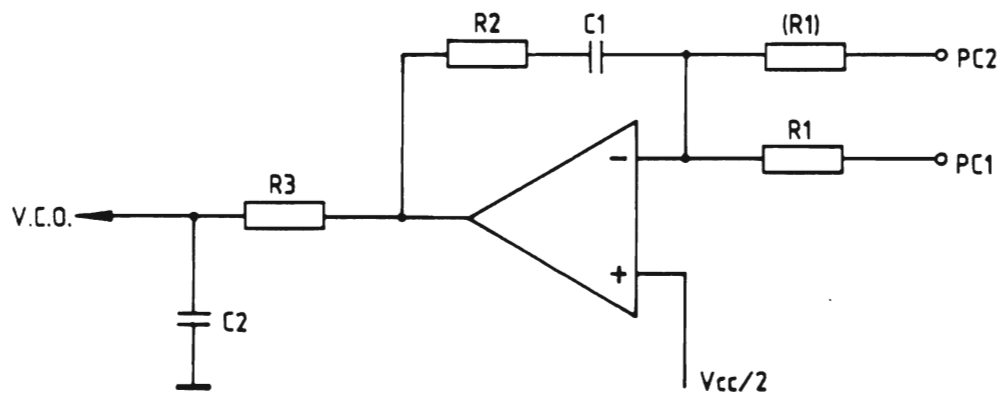


FIG. 4. LOOP FILTER TYPE A.

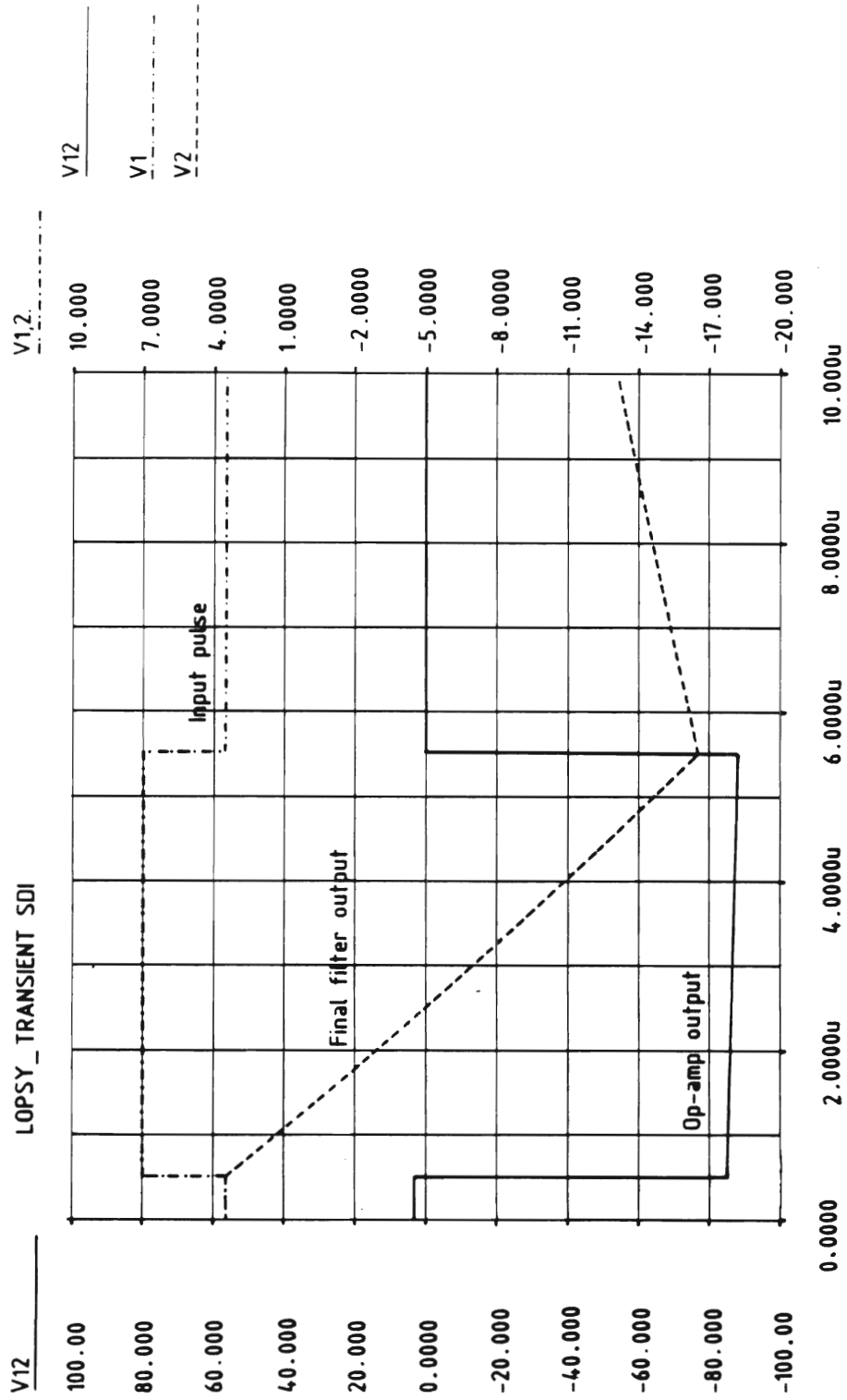


FIG. 5. TYPE A FILTER RESPONSE TO PC2 SIGNAL.

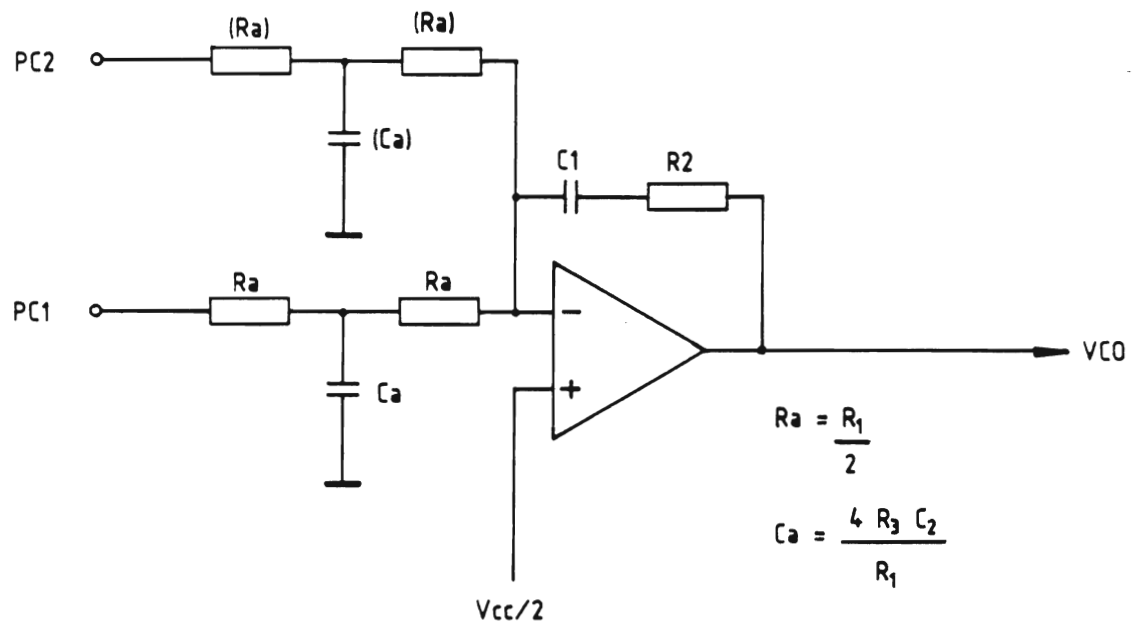
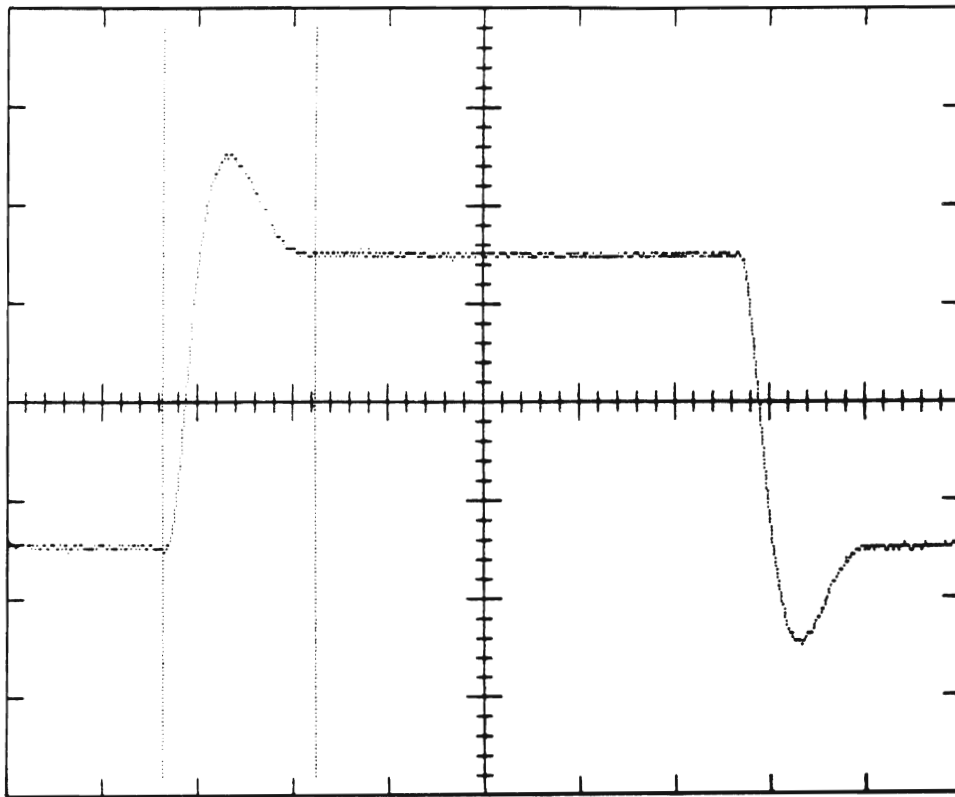


FIG. 6. LOOP FILTER TYPE B.



Loop filter output : frequency step = 10 MHz
settling time = 760 μ sec

FIG. 8. WORKED EXAMPLE 1. SWITCHING WAVEFORM.

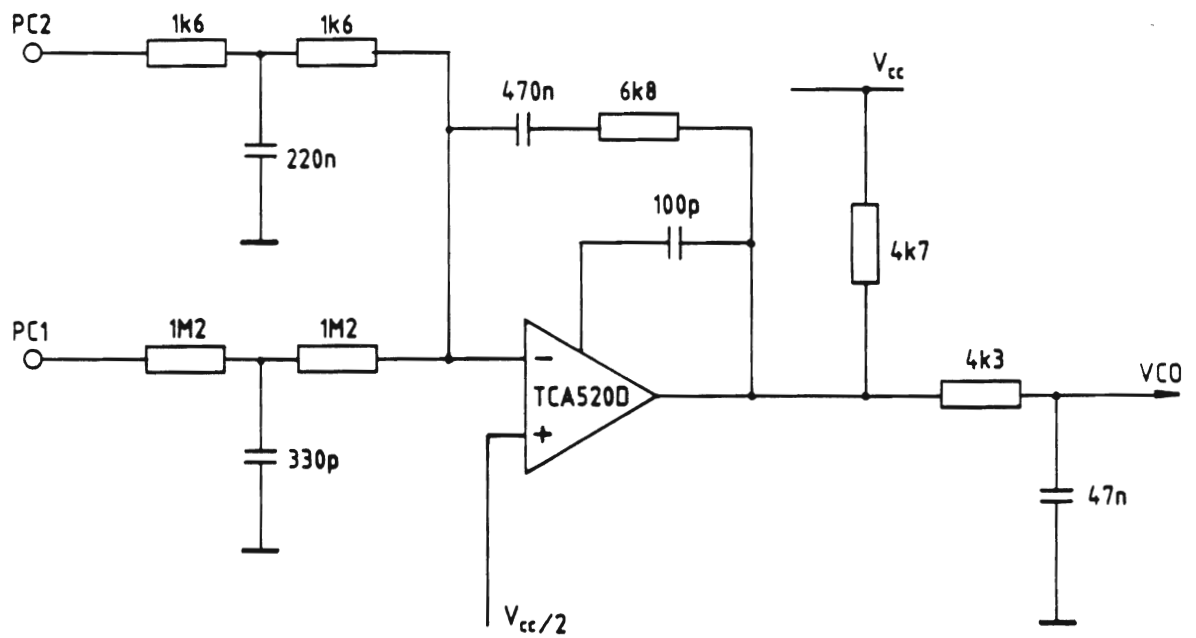


FIG. 9. WORKED EXAMPLE 2. LOOP FILTER CIRCUIT DIAGRAM.

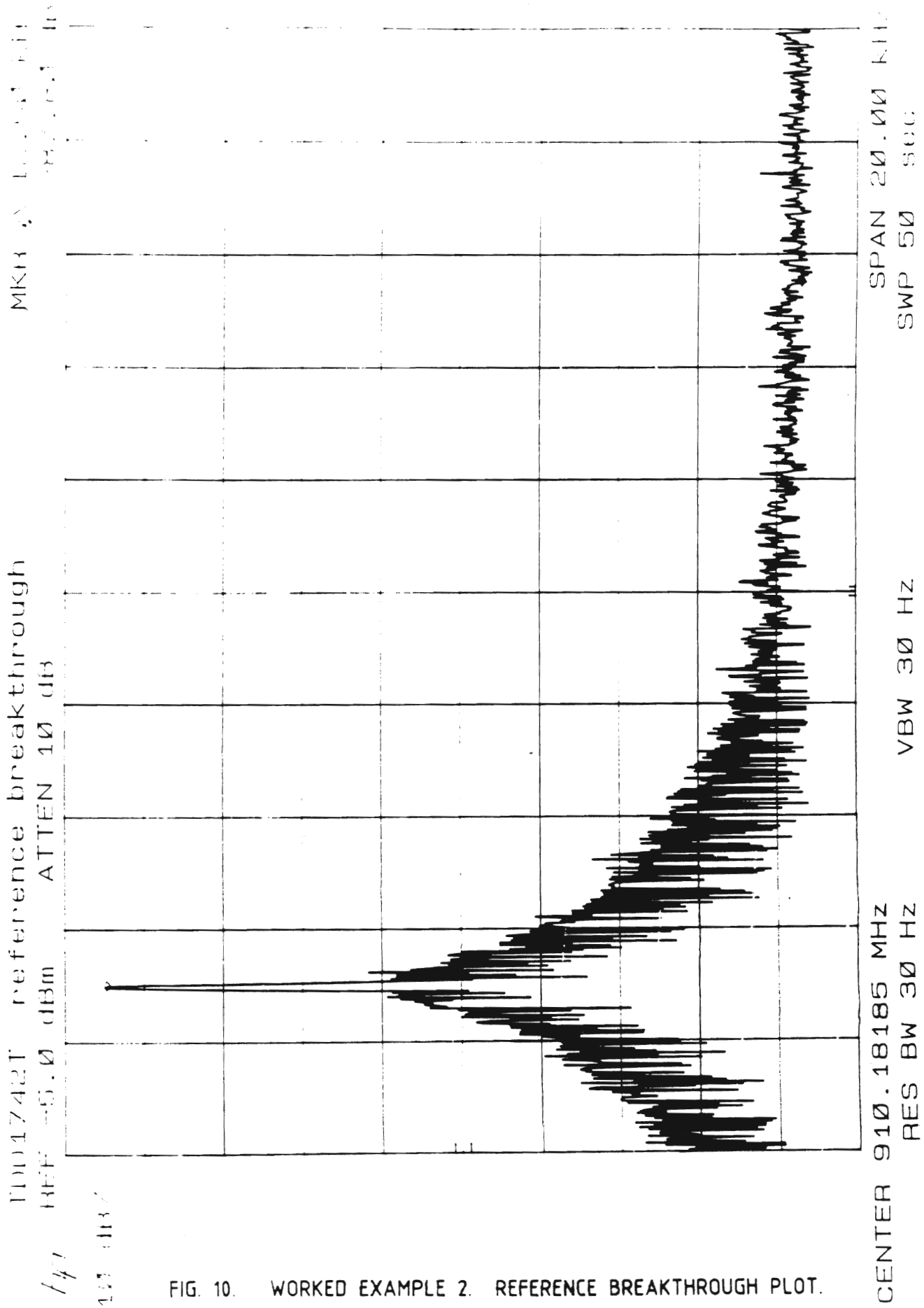


FIG. 10. WORKED EXAMPLE 2. REFERENCE BREAKTHROUGH PLOT.

